METHODS OF THINNING A SILICON WAFER USING HF AND OZONE

[0001] This application is a Continuation-in-Part of U.S. Patent Application Serial No. 09/621,028, filed July 21, 2000 and now pending, which is: a Continuation-in-Part of Serial No. 60/145,350 filed July 23, 1999; a Continuation-in-Part of Serial No. 08/853,649, filed May 9, 1997 and now U.S. Patent No. 6,240,933; and a Continuation-in-Part and U.S. National Phase Application of International Application PCT/US99/08516, filed April 16, 1999, which in turn is a Continuation-in-Part of U.S. Patent Application Serial Nos. 60/125,304 filed March 19, 1999; 60/099,067 filed September 3, 1998; and 09/061,318, filed April 16, 1998. These applications are also incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] Silicon wafer thinning is an important step in the manufacture of semiconductor devices and micro-electro mechanical systems (MEMS). Wafer thinning is vital because it aids in preventing heat build-up in the wafer during manufacture and use, and also makes the wafer easier to handle and less expensive to package.

[0003] Traditionally, the wafer thinning process has been performed by grinding and polishing operations commonly referred to as "backgrinding," or by using solutions containing strong oxidizers such as nitric acid (HNO_3) and/or hydrofluoric acid (HF). These two processes are also often combined, because the mechanical grinding operation induces a significant amount of stress in the silicon

surface. This stress may be alleviated by chemical etching, which removes the stressed and damaged layer. The chemical reactions for this process generally proceed as follows:

$$Si + 2HNO_3 \text{ --> } SiO_2 + 2NO_2 \text{ (silicon oxidation)}$$

$$4HF + SiO_2 \text{ --> } SiF_4 + 2H_2O \text{ (dissolution of silicon dioxide)}$$

[0004] From these reactions, it is apparent that the silicon removal mechanism is the formation of silicon dioxide by exposure to an oxidizing agent (HNO_3), followed by the reaction of the silicon dioxide with fluorine to form silicon tetrafluoride (SiF_4), which can be dissolved in an aqueous carrier or evolved as a gas. While numerous oxidizing agents have been experimented with, there appear to be few alternatives to fluorine for the reaction to effectively proceed.

[0005] One problem with this process is that it is difficult to control, due to the consumption of reactants and the evolution of nitrous oxides which dissolve into the etchant solution, thereby "poisoning" the bath by saturation, which will affect subsequent etches. The process also requires large volumes of expensive process chemicals, involves a great deal of hazardous waste, and is difficult to control to the extent required in order to deliver optimal etch uniformity.

[0006] Alternative silicon etchants include caustic solutions such as potassium hydroxide or sodium hydroxide, or fluorine plasma chemistries such as SiF_6. The two primary classes of silicon etchants can thus be classed as either aqueous chemistries applied in the liquid state (e.g., HNO_3, HF, or caustics), or

fluorine plasmas. Each of these process categories has certain applications and limitations.

[0007] In the case of aqueous chemistries, limitations include the cost of the chemicals, the need for significant amounts of water for rinsing, the creation of large volumes of waste (chemical and rinse water), and the inability to deliver the etchant into small geometries, which are common in semiconductor devices and MEMS devices. In general, caustics are not favored in the semiconductor industry, due to commonly known problems associated with mobile ion contamination. This is especially true of elements such as Na and K.

[0008] In the case of plasma chemistries, the cost of the processing equipment and supporting hardware (e.g., vacuum pumps) can be quite high. Many plasma processes are designed to deliver an anisotropic etch profile. While this has many desirable features, it has a tendency to create very sharp corners on system geometries, which can lead to device breakdown. Many of these systems are also designed for single-wafer processing, which can prove detrimental, depending on throughput requirements. Additionally, plasmas are relatively expensive, dirty, and are not configured for the removal of several hundred microns of silicon as required in a wafer thinning operation.

[0009] Thus, there is a need for an improved method of thinning silicon wafers used in semiconductor devices and/or MEMS devices.

SUMMARY OF THE INVENTION

[0010] The present invention is directed to a method of thinning a silicon wafer using ozone and HF. The ozone oxidizes one or more layers of silicon on the wafer surface, and the HF etches away the oxidized silicon layer, thereby thinning the wafer.

[0011] In a first aspect, ozone gas is delivered into a process chamber containing a silicon wafer. HF vapor is delivered into the process chamber, either simultaneously with the ozone gas, or after the ozone gas delivery has begun. The HF vapor is preferably delivered via a carrier gas, which may also be ozone gas, or may be an inert gas. The HF vapor etches the oxidized silicon layer to thin the wafer.

[0012] In another aspect, ozone gas is delivered into a process chamber containing a silicon wafer. Anhydrous HF gas is delivered into the process chamber while deionized (DI) water is sprayed onto a surface of the wafer. The anhydrous HF gas dissolves into the DI water, which may form a microscopic aqueous boundary layer on the wafer surface, and etches the oxidized silicon layer on the wafer surface to thin the wafer. The wafer may be rinsed after the etching process is completed.

[0013] In another aspect, ozone gas is delivered into a process chamber containing a silicon wafer in order to oxidize a layer of silicon on the wafer into SiO_2. HF is delivered into the process chamber to react with the SiO_2 layer and convert the SiO_2 layer into SiF_4. The SiF_4 is then removed to thin the wafer.

[0014] Any of the described processes may be combined and/or repeated one or more times to achieve optimal results. Other features and advantages of the invention will appear hereinafter. The invention resides as well in sub-combinations of the features described, as well as in the system or apparatus shown in the drawings and described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Fig. 1 is a perspective view of a wafer processing system.

[0016] Fig. 2 is a front view of the wafer processing system illustrated in Fig. 1.

[0017] Fig. 3 is a schematic diagram of a wafer processing system that may be used to perform the wafer thinning methods of the preferred embodiments.

DETAILED OF DESCRIPTION OF THE DRAWINGS

[0018] In a method of thinning a silicon wafer, ozone gas or vapor is delivered into a process chamber containing a silicon wafer. The ozone oxidizes one or more layers of silicon on the wafer surface. HF etches away the oxidized silicon layer, thereby thinning the wafer. The HF may be provided in vapor form, anhydrous gas form, or aqueous form. The HF may be delivered simultaneously with, or shortly following, the delivery of the ozone into the process chamber. Other steps and features described below may be advantageous but are not necessarily essential to the invention.

[0019] The methods described herein for processing silicon wafers, which provide support for semiconductor devices and/or MEMS devices, may be performed in a variety of processing systems. Conventional semiconductor wafer processing systems, for example, may be used to process the silicon wafers. Moreover, one or more processing systems may be used to perform the various processing steps described herein. Thus, the processing system 10 described below is only one example of a processing system that could be used to process silicon wafers according to the claimed methods.

[0020] Turning now in detail to the drawings, as shown in Figs. 1 and 2, a wafer processing system 10 preferably includes an enclosure 12 to maintain and control clean airflow and reduce contamination of wafers being processed in the processing system 10. An input/output station 14 at the front of the system 10 allows wafers 60 to be loaded and unloaded to and from the system 10. An indexer 16, or other temporary wafer storage station, is preferably provided adjacent to the input/output station 14.

[0021] The system 10 may be divided into an interface section 24 and a process section 26. These sections may be separated by a partition having a door opening. The interface section 24 includes the input/output station 14 and the indexer 16. The process section 26 includes one or more process stations 30, with each process station 30 including a wafer processor. The interface section 24 also preferably includes a process robot 22 for moving wafers 60 between the indexer 16 and the processor unit. A control panel 28 may be provided on the enclosure 12, to

allow instructions or programming to be input into a computer controller 32 which controls the system 10.

[0022] The wafers 60 may be provided in open carriers, cassettes, or trays, and handled as described in U.S. Patent Nos. 6,279,724 or 5,664,337, both incorporated herein by reference. Alternatively, the wafers 60 may be provided within sealed pods or containers which are unsealed at a docking station, as described in U.S. Patent No. 6,447,232 or U.S. Patent Application Serial Nos. 09/612,009 or 10/200,074, each incorporated herein by reference.

[0023] The processors 30 in the processing system 10 may be batch processors or single wafer processors (e.g., as described in U.S. Patent No. 6,423,642, incorporated herein by reference), similar to those used in existing semiconductor wafer processing systems. Several variations of batch processors and/or single wafers processors may be used. For example, a batch processor with a 25-wafer capacity, or alternatively, a 50-wafer capacity, may be used.

[0024] The processors 30 preferably each include a rotatable wafer holder or rotor, so that the wafers 60 may be rotated during processing. Rotation of the wafers 60 may be used for distributing process fluids evenly across the wafer surfaces, for spin-drying the wafers 60, or for other reasons, as is common in the processing of semiconductor wafers.

[0025] Fig. 3 is a schematic flow diagram of a preferred wafer processing system. In operation, one or more wafers 60 are loaded into a wafer holder or rotor in a process chamber 45, which may comprise a batch processor or a single wafer

processor. The wafers 60 may be loaded manually, by a robot, or by another suitable loading device. The wafers 60 may be handled or contacted directly by the robot or rotor. Alternatively, the wafers 60 may be handled within a carrier tray or cassette, which is placed into the rotor or other holder.

[0026] Once the wafers 60 are loaded into the processor, the process chamber 45 is preferably closed, and may optionally form a fluid-tight seal. Ozone (O_3) gas is then provided into the process chamber from an ozone source 40. The ozone gas may be delivered into the process chamber 45 via a manifold 68, nozzles, or another suitable device. The ozone gas preferably fills the process chamber 45 to form an ozone environment. The ozone may alternatively be mixed with HF vapor before entering the process chamber 45, and/or may be used as a carrier gas for HF vapor, as described below.

[0027] The ozone oxidizes one or more layers of silicon on the wafers 60, converting the silicon to silicon dioxide (SiO_2). Pure oxygen (O_2) may alternatively be used to convert the silicon layer into silicon dioxide. The silicon oxidizing reaction generally proceeds as follows:

$$Si + 2O_3 \rightarrow SiO_2 + 2O_2$$

Or $$Si + O_2 \rightarrow SiO_2$$

[0028] HF vapor is provided into the process chamber 45 to etch the oxidized silicon layer. To generate the HF vapor, HF liquid may be provided in an HF fill vessel 62, and then pumped into an HF vaporizer 61 with a pump 64. The HF vaporizer 61 is preferably connected to a heat exchanger 66, which may provide

heat to the HF vaporizer 61 to convert the HF liquid into HF vapor. In general, the vapor may be generated as described in U.S. Patent No. 6,162,734, incorporated herein by reference. The generated HF vapor is provided into the process chamber via the vapor delivery manifold 68, or another suitable device.

[0029] The HF vapor may be delivered into the process chamber 45 after the ozone begins to enter the process chamber 45, or it may be mixed with the ozone before entering the process chamber 45. The key element is that the silicon surface of a wafer 60 is oxidized by the ozone, and the oxidized surface is then etched by the HF vapor. The wafers 60 may be rotated in the rotor to promote homogenous mixing and chemical distribution on the wafer surfaces.

[0030] The HF vapor is preferably mixed with a carrier gas, such as nitrogen (N_2) gas, for delivering the HF vapor into the process chamber 45, as is common in the semiconductor wafer manufacturing industry. N_2 gas, or a gas with similar properties, may also be delivered to the process chamber 45 after the wafers 60 are processed, in order to purge any remaining HF vapor from the process chamber 45 before the chamber door is opened. The use of HF vapor in conjunction with a carrier gas, as well as possible configurations for generating HF vapor for use in etch applications, is described in U.S. Patent Nos. 5,954,911 and 6,162,735, incorporated herein by reference.

[0031] Other gasses, such as compressed dry air, oxygen, and CO_2, could alternatively be used as a carrier gas. Ozone gas may also be used as the carrier gas, and may be preferable in some applications, since it is integral to the oxidizing

process, and would minimize the dilution effects of using an inert gas, such as nitrogen. The carrier gas is preferably delivered from a gas source 80 into gas manifold 82. The carrier gas preferably exits the manifold 82 and is delivered through a mass flow controller (MFC) 84 into the HF vaporizer 61, and to any other desired system components. The MFC is preferably an electronic device that controls the mass of the carrier gas that flows to the other system components.

[0032] The carrier gas passes through the HF vaporizer 61, where it entrains the HF vapors and carries them to the process chamber 45 to react with the oxidized silicon layer, or other material to be etched. To generate the HF vapor, the carrier gas may be bubbled through the HF solution in the HF vaporizer 61, or may be flowed across the surface or the HF solution, thereby becoming enriched in HF and water vapor. Alternatively, the HF vapor may be generated by heating or sonically vaporizing the HF solution.

[0033] When the HF vapor enters the process chamber 45, it may form a visible condensate film on the surface of the wafers 60. Regardless of whether a visible condensate film is formed, a microscopic aqueous boundary layer, which is condensed from the gas/vapor phase environment in the process chamber 45, is preferably formed on the wafer surface. HF vapor and/or ozone are present in the microscopic boundary layer as dissolved or diffused species from the surrounding gas/vapor environment.

[0034] There is a significant distinction between a microscopic boundary layer and a macroscopic boundary layer, which is often used in semiconductor wafer

cleaning operations (as opposed to thinning operations). The microscopic boundary layer is a condensed phase layer formed from a vapor/gas environment, whereas a macroscopic boundary layer is a visible liquid formed on the wafer surface by spraying or otherwise delivering an aqueous solution onto the wafer surface.

[0035] The objective in wafer thinning is to form a microscopic liquid boundary layer on the wafer surface that has condensed from the gas/vapor phase. Because the boundary layer is microscopic, the wafer surface never becomes "wet" in the conventional wafer-cleaning sense. Thus, rinsing and drying are typically not required in the wafer thinning operations described herein, whereas rinsing and drying are typically required in semiconductor cleaning operations. Rinsing and drying may optionally be used, however, after the etching process is completed, to remove any contaminants from the wafer surface.

[0036] The HF vapor enters the process chamber and begins to etch the silicon dioxide film on the wafers 60. Fresh ozone gas is preferably continuously supplied into the process chamber 45 during the etching process, in order to continually oxidize the exposed silicon surface of the wafer. The HF vapor reacts with the silicon dioxide to form silicon tetrafluoride (SiF_4), which may then be evolved as a gas and removed via a system exhaust, or may be dissolved in an aqueous carrier liquid. The silicon dioxide dissolution reaction generally proceeds as follows:

$$4HF + SiO_2 \text{ -->} SiF_4 + 2H_2O$$

[0037] Thus, the entire oxidizing and etching process is generally as follows:

$$Si + 2O_3 \text{ --> } SiO_2 + 2O_2$$

Or $$Si + O_2 \text{ --> } SiO_2$$

$$4HF + SiO_2 \text{ -->} SiF_4 + 2H_2O$$

[0038] In a typical wafer thinning application, a silicon wafer is etched from a thickness of 500-1000 microns down to 50-100 microns, preferably from 650-850 microns down to 65-85 microns. Accordingly, the HF vapor preferably etches silicon at a rate of 1000 Å/min or higher, more preferably 5000 to 10,000 Å/min or higher (1 micron = 10,000 Å). The silicon surface is continuously etched in the presence of HF vapor and ozone until the desired wafer thickness is achieved. Because vaporous HF is used, no rinsing or drying step is required, although rinsing and drying may be used if desired. Additionally, only a minimal amount of chemical is required to thin the wafers, and a relatively small amount of chemical must therefore be disposed of, which is ecologically beneficial.

[0039] In an alternative embodiment, HF is delivered into the ozone-filled process chamber as an anhydrous gas. Anhydrous HF gas does not generally produce a significant etch rate on silicon dioxide films. In order for the etch rate to become significant for most applications, the anhydrous HF gas must be mixed with water so that it is no longer anhydrous.. The presence of water vapor appears to catalyze the reaction. The absence of water renders the HF gas essentially inert in regards to silicon dioxide. Thus, the anhydrous HF gas is preferably either mixed with water prior to delivery to the wafer surface, or mixed with an aqueous layer on the wafer surface.

[0040] In a preferred method, deionized (DI) water, maintained at a controlled temperature, is sprayed onto a wafer surface simultaneously with the delivery of anhydrous HF gas into the process chamber. The anhydrous HF gas dissolves in the DI water, causing the anhydrous HF gas to become aggressive toward the silicon dioxide on the wafer surface. The anhydrous HF gas, mixed with water, etches the silicon dioxide film on the wafer surface. The etch product (SiF_4) may then be evolved as a gas and removed via a system exhaust, or may be dissolved in an aqueous carrier liquid

[0041] The anhydrous HF gas may alternatively be bubbled into water, or mixed with a water vapor or aerosol, within the processing chamber, or prior to entering the processing chamber. In the latter cases, HF vapor is generated by mixing anhydrous HF gas with water vapor. The anhydrous HF gas may also be mixed with ozone before being delivered into the process chamber. Regardless of how the anhydrous HF gas and the ozone enter the process chamber, both HF and ozone are preferably present in the microscopic aqueous boundary layer at the wafer surface, as described above.

[0042] In another embodiment, HF may be delivered into the process chamber as an aqueous solution. The HF solution may have other additives such as ammonium fluoride as a buffer, organic solvents such as ethylene glycol to help promote surface wetting and control ionization, or other commonly used additives. HF and water, however, are preferably the key components to the solution. The other processing steps are performed as described above to thin the wafers.

[0043] While the primary focus of the present invention is the use of ozone and HF for the purpose of etching silicon to thin silicon wafers, it is acknowledged that other gas mixtures and additives might also be used to accomplish specific cleaning purposes. For example, alcohol mixtures may be used to help control etch selectivity between various film types exposed to the etchant vapors. HCl may be used to enhance the removal of metal contaminants.

[0044] Additionally, several options are viable to conclude the etch processes described herein. For example, a rinse with DI water or another suitable agent may be performed to quench the process. Additionally, the delivery of HF vapor may be continued without ozone in order to ensure an oxide-free hydrophobic silicon surface, or conversely, the delivery of ozone may be continued without HF vapor to ensure an oxidized hydrophilic silicon dioxide surface. Other processes may also be performed to meet the needs of a given application.

[0045] The present invention is a method of etching silicon in wafer thinning applications using less expensive and more controllable techniques than those currently practiced. In order to accomplish this, ozone gas is used as a silicon oxidizer, and HF vapor or gas is used to etch the oxidized silicon.

[0046] Potential benefits of the methods described herein are that they:

(a) minimize chemical consumption and waste generation in silicon wafer thinning applications;

(b) eliminate the requirement for a post-etch rinse (in some embodiments, such as the vapor phase reaction);

(c) readily lend themselves to a single-side application, where the non-processed side of the wafer would only need to be protected from vapor species (which is much more easily accomplished than is protection from liquid reactants);

(d) lend themselves equally well to batch processing;

(e) create a final wafer surface state (oxidized or bare silicon) that can be easily dictated by process configuration

(f) may be integrated with backgrind or plasma etch processes to remove a portion of the material in conventional grinding operations and then use the ozone/HF process to relieve stresses; and

(g) have the potential to etch other materials, such as gallium arsenide.

[0047] The essential elements of the system 10 as shown in Fig. 3 are the HF source 61, the ozone source 40, and the process chamber 45. The other elements shown in Fig. 3 may also be used in combination with these essential elements.

[0048] While the term wafer as used here generally refers to silicon or semiconductor wafers, it also encompasses similar flat media articles or workpieces which may not be silicon or a semiconductor, but which may be etched or thinned as described.

[0049] While embodiments and applications of the present invention have been shown and described, it will be apparent to one skilled in the art that other

modifications are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except by the following claims and their equivalents.